Register Allocation for the Intel(R) Itanium(R) Processor

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Johannes Kepler Universität Linz, Raum HS 14

Abstract:
Graph-coloring based register allocators have been implemented in commercial and research compilers since Gregory Chaitin’s and colleagues pioneering work in the early 1980’s. The Itanium processor is commercially available since 2001. This talk sketches the history of graph-coloring based allocators, gives background on the Itanium architecture and shows how to extend classical allocators for Itanium with its support for predication, control- and data speculation and dynamic register stack. A general problem of coloring allocators is that they are slow for large candidate sets. The presentation will discuss methods to handle allocation problems of any size efficiently.

Gerolf Hoflehner is a Research Scientist in the Intel Microprocessor Research Lab, Santa Clara. He worked on the optimizing Intel Itanium backend as developer and project lead from 1999 - 2008. Prior to joining Intel he worked in compiler development teams at Siemens (Munich), Pyramid (San Jose), and Sun Micro (Menlo Park). He has a Diplom in Mathematics from the Technical University Munich, Germany.

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