The department consists of the following institutes:

- Application Oriented Knowledge Processing (FAW)
- Bioinformatics
- Computational Perception
- Computer Architecture
- Computer Graphics
- Formal Models and Verification
- Networks and Security
- Integrated Circuits
- Pervasive Computing
- Software Systems Engineering
- System Software
- Telecooperation
- Signal Processing

ÖGI-Sekretariat, z.Hd. Frau Monika Neubauer
Johannes Kepler Universität Linz, Altenberger Straße 69, A-4040 Linz, Austria
oegi-office@faw.jku.at              http://oegi.ocg.at

The Department of Computer Science of Johannes Kepler University Linz\(^1\) together with the Austrian Society of Computer Science (ÖGI) invites to the following talk:

**Clifford Wolf**

**Formal Verification of Verilog HDL with Yosys-SMTBMC and SymbiYosys**

March 6th, 2017,
Talk 13:00 – 14:00
Discussion 14:00 – 15:00

Johannes Kepler University Linz, Science Park 2 S2 Z74

Abstract:
Yosys is a free and open source Verilog synthesis tool and more. In this presentation we discuss Yosys-SMTBMC, a Yosys-based formal verification flow that can use any SMT-LIB2 solver as back-end engine, and SymbiYosys, a uniform front-end for various Yosys-based formal flows, including Yosys-SMTBMC and flows utilising AIGER-based engines.

About the Speaker:
Clifford Wolf develops open source software, has been teaching at Metalab and collaborates and publishes with the Institute of Computer Technology, of the Vienna University of Technology. He is particularly interested in developing high quality open source solutions for Electronic Design Automation (EDA), which are software tools for industrial hardware design.

Host: *Prof. Dr. Armin Biere*
    Institute of Formal Models and Verification